MULTI-CORE PROCESSOR BASED ON LEON3-FT IP CORE (LEON3-FT-MP)

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1 ABSTRACT

This paper summarizes the development, verification and validation of a multi-core processor system (LEON3-FT-MP) based on the LEON3-FT IP core. The work was performed by Gaisler Research under ESA contract during the period from September 2005 to April 2006. The project is preparation for the next generation ESA microprocessor called GINA (GIga Instruction Architecture) which has ambition to provide 1,000 MIPS/MFLOPS in a single device. Verification and validation platform consisting of multi-processing system based on LEON3-FT and GRFPU IP cores was successfully developed. Fault-tolerant and multi-processing capabilities of LEON3-FT, GRFPU and additional IP cores from Gaisler Research have been demonstrated and validated.

2 INTRODUCTION

The main objective of this work was to develop a multi-processing system based on LEON3-FT and GRFPU IP-cores [1] satisfying the requirements on the next generation ESA microprocessor (GINA). The proposed system is functionally comparable to the configuration which is believed to be used for future ASIC implementations of GINA architecture. The proposed LEON3-FT-MP architecture consists of 4 LEON3-FT CPU cores each one configured with GRFPU floating point unit and SRMMU memory management unit. The proposed multi-processor architecture offers performance of > 1,000 MIPS/MFLOPS on a 0.13 CMOS process meeting the requirements on the next generation of ESA microprocessor.

The verification and validation focused on fault-tolerant and multi-processing capabilities of LEON3-FT and GRFPU IP cores. LEON3-FT and GRFPU IP cores were configured to enable SEU protection for all on-chip memories including register files and caches. Verification of fault-tolerant capabilities was done by inserting errors on VHDL level. During system validation errors were inserted in all on-chip memories using GRMON error injection feature [2], effectively emulating SEU testing.

eCos and RTEMS operating systems [3, 4] have been adapted and used to demonstrate multi-processing capabilities of the LEON3-FT-MP system.

An FPGA validation board based on Virtex-4 LX200 FPGA was developed and served as validation platform.

3 ARCHITECTURE

3.1 Overview

The LEON3-FT-MP consists of four LEON3-FT processor cores and a set of additional IP cores. The architecture is based on two AMBA AHB buses [5]; a high-speed bus connecting the processor cores and the SDRAM memory controller, and a low-speed bus for communications IP cores (figure 1). The on-chip communications interfaces include four spacewire links, one ethernet 10/ 100 Mbit MAC, two CAN-2.0 interfaces, one 32-bit PCI interface and four serial UARTs. For debugging, both serial, JTAG and Ethernet debug DSU interfaces are provided. Legacy cores such as an interrupt controller and timer unit is provided to support the hosting of common operating systems. A 32-bit I/O port is provided for controlling of external devices.

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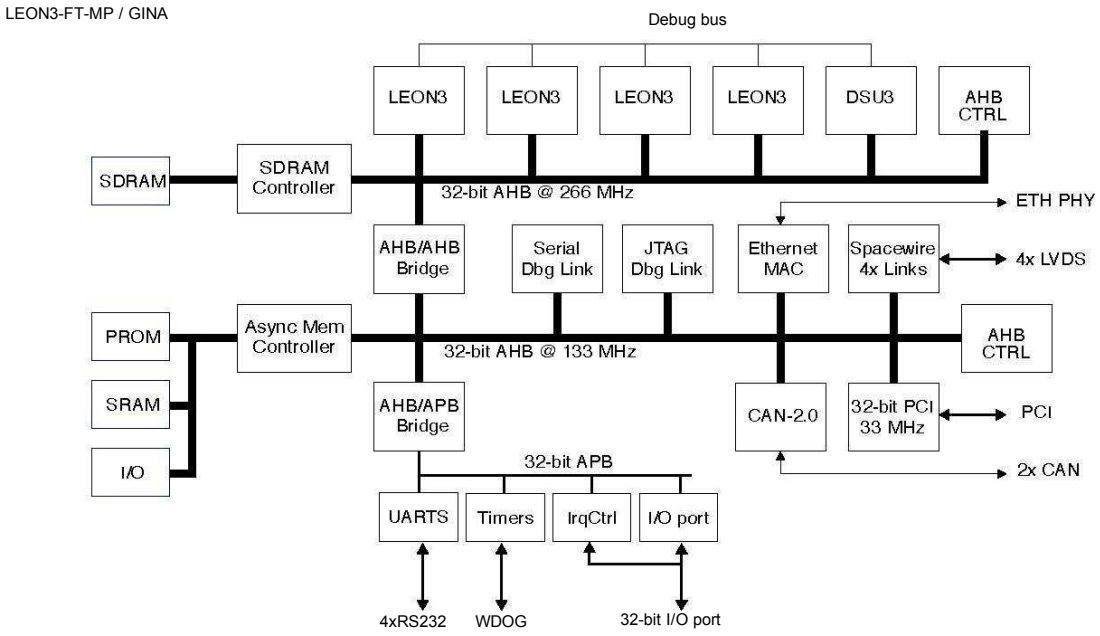

Figure 1. LEON3-FT-MP block diagram

3.1.1 AMBA Bus Architecture

The LEON3-FT-MP design consists of two AMBA AHB buses; a high-speed bus connecting the processor cores and the SDRAM memory controller, and a low-speed bus for communications IP cores. The high-speed bus connects the processor cores to the external SDRAM controller, and is clocked at the same frequency as the LEON3 processors. On a typical 0.13 CMOS process the target frequency would be 266 MHz. The low-speed bus, clocked at half the frequency of high-speed bus (133 MHz), connects all on-chip communications interfaces. High-speed bus provides high bandwidth between CPU cores and the external memory (SDRAM). To maximize bus bandwidth utilization on the high-speed bus all communication IP cores with high-latency access are placed on the low-speed bus and accessed through the bridge. High latency is hidden through use of AMBA split transfers and FIFOs in the AHB/ AHB bridge.

3.1.2 LEON3FT SPARC V8 processor

LEON3 is a 32-bit processor core conforming to the IEEE-1754 (SPARC V8) architecture [6]. The LEON3 core has the following main features: 7-stage pipeline with Harvard architecture, separate instruction and data caches, hardware multiplier and divider, on-chip debug support and multi-processor extensions.

The processor configuration in LEON3-FT-MP consists of 16 + 16 Kbyte I/D cache with 2-set LRU replacement. The SPARC Reference Memory Management Unit (SRMMU) is enabled and configured with 16 + 16 separate I/D TLB entries and LRU replacement. Each CPU core is configured to use GRFPU as floating-point unit. The debug interface is enabled with an instruction trace buffer of 2 Kbytes.

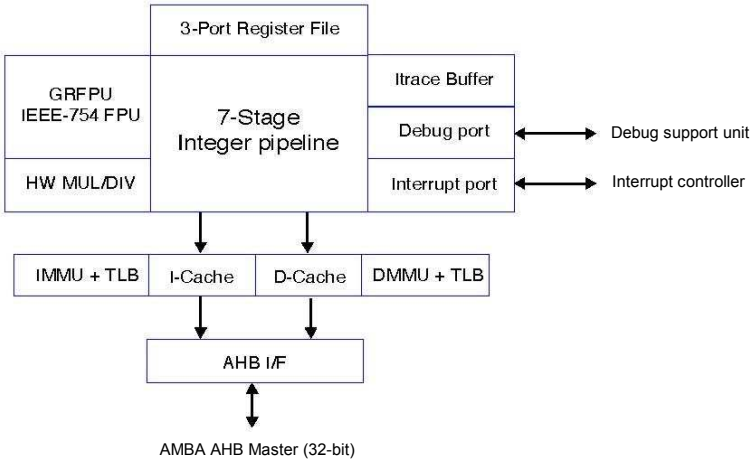

Figure 2. LEON3-FT processor core block diagram

LEON3 CPUs are debugged through the LEON3 Debug Support Unit (DSU3). Each CPU can be controlled and debugged individually. DSU3 provides access to each CPUs internal registers and instruction trace buffer. Conditions for entering debug mode (e.g. on breakpoint hit) can be defined individually for each CPU. DSU3 includes buffer for AHB tracing.

3.1.3 Memory interfaces

The external memory is interfaced in two places; the high-speed bus is connected to an SDRAM controller while the low-speed bus is connected to a combined PROM/SRAM/IO controller. The SDRAM interface uses 32-bit data and 16-bit Reed-Solomon ECC.

The combined controller uses 8- or 32-bit data with 7-bit BCH ECC.

3.1.4 Communications IP cores

Spacewire links

The LEON3-FT-MP includes four Spacewire links. Each link is controlled separately through the APB bus, and transfers received and transmitted data through DMA transfer. Two of the Spacewire links are configured with Remote Memory Access Protocol (RMAP) support in hardware. All links can operate up to 400 Mbit/s.

CAN interface

A dual CAN-2.0 interface is provided in form of an Philips SJA1000-compatible CAN core.

Ethernet

An ethernet interface based on Gaisler Research's GRETH ethernet MAC is included. The MAC has a built-in debug communication protocol and provides debug communication link (EDCL). The EDCL allows debugging and downloading of applications with up to 50 Mbit/s.

PCI Interface

A 32-bit PCI interface is provided, based on the GRPCI core. The PCI operates at 33 MHz and supports Master, Target and System Controller operations. The PCI core includes one DMA channel for autonomous data transfers, but can also be accessed directly by any AHB master. A separate PCI arbiter provides PCI arbitration and bus control.

UARTs

Four UARTs can be configured in the design. The UARTs are configured with flow-control, 16 byte transmit and receive FIFOs.

General purpose I/O port

A general purpose I/O port (GPIO) is provided in the design. The port is 32 bits wide, and each bit can be dynamically configured as input or output. GPIO can route external inputs to 15 APB interrupt lines allowing external devices to generate interrupts.

3.1.5 Other IP-cores

Timer unit

The timer unit consists of a common 16-bit scaler and 7 individual timers. The timers can work in periodical or on-shot mode. Timer 7 is configured as a watchdog. The timers use individual interrupts.

Interrupt controller

The interrupt controller handles up to 15 interrupts in two priority levels. The interrupt are automatically assigned and routed to the controller through the use of the GRLIB's AMBA plug&play system. Interrupt controller contains one watchdog per CPU.

3.2 Software

eCos and RTEMS have been adapted to support multi-processing capabilities of the LEON3FT-MP system. Both operating systems have a test suites which were used during hardware and software validation.

3.2.1 eCos

eCos is real-time operating system whose key features is modular design and configuration tool allowing users to customise eCos according to their specific and precise application requirements. eCos provides all the functionality required for general embedded applications providing features such as full preemptability, synchronizations primitives, scheduling policies, device drivers and memory management. Gaisler Research has developed and contributed the LEON2 and LEON3 ports of eCos.

eCOS supports true symmetric multi-processing (SMP). A multi-threaded application is automatically distributed on the available processor nodes, without need for message passing or knowledge about the underlying architecture.

3.2.2 RTEMS

RTEMS (Real-Time Executive for Multiprocessor Systems) is a real-time operating system designed for deeply embedded systems. RTEMS is widely used in space applications. RTEMS provides features such as multitasking, priority based preemptive scheduling, intertask communication and synchronization and interrupt management.

RTEMS uses message passing between CPUs through shared memory. In a multi-processor system each CPU executes its own image and communicates with other CPUs by message passing through shared memory buffer. This is a robust approach but requires software partitioning to fit the underlying hardware architecture.

4 LEON3-FT-MP INTEGRATION

4.1 System-On-Chip (SOC) Design

LEON3-FT-MP SOC design was straight-forward due to GRLIB's plug&play method [7] to connect and configure GRLIB IP cores. The IP cores are centered around AMBA on-chip bus. IP cores are configured through VHDL generics defining memory mapping, interrupt routing or any other core specific configuration options without need to modify any global resources. GRLIB support generation of simulation and synthesis scripts in completely automatic manner.

4.2 Verification

The verification of the LEON3-FT-MP system focused on the fault-tolerant and multi-processing capabilities of the LEON3-FT and GRFPU IP cores. The verification was performed by means of VHDL simulations using LEON3/GRLIB test bench, GRFPU test bench and SPARC V8 validation test suite. The fault-tolerance capabilities were tested by running all tests with built-in error injection functions. All tests were successfully run with and without error injection.

Functionality of eCos and RTEMS multi-processing extension was verified by running test suites on GRSIM behavioral simulator.

5 FPGA PROTOTYPING

5.1 GR-CPCI-XC4VLX200 FPGA board

An FPGA board incorporating high-capacity Virtex-4 FPGA has been developed and served as platform for hardware and software validation. The board (GR-CPCI-XC4VLX200) provided capability to host LEON3-FT-MP system and all necessary interfaces.

The features of the GR-CPCI-XC4VLX200 board include:

- Compact-PCI plug-in form factor
- Virtex-4 XCVLX200-FG1513-10 FPGA
- 16 Mbyte FLASH PROM
- 1 standard SO-DIMM socket for up to 512 Mbyte SDRAM

- Ethernet PHY 10/100 Mbit transceiver
- Standard RS-232 UART port
- 120-pins memory and custom I/O expansion connectors
- CPCI system controller (clock distribution & PCI arbitration)

5.2 FPGA Synthesis

The complete 4-cpu system was synthesized and fitted on Virtex-4 FPGA device of the GR-CPCIXC4VLX200 board. The design used 70% of available logic resources and run at 40 MHz. Maximum clock frequency was limited due to large area utilization (a single CPU system run at 80 MHz). FPGA synthesis tools had significant difficulties with LEON3-FT-MP design which resulted in internal errors caused by the large size of the design. Therefore, the design had to be partitioned and synthesized in blocks.

6 SYSTEM VALIDATION

The system validation was processor driven and focused on the fault-tolerant and multi-processing capabilities of the LEON3-FT IP-core. The system validation was based on the GR-CPCI-XC4VLX200 board, GRMON debug monitor and LEON3 software environment.

Multi-processing capabilities of the system were validated by running eCos and RTEMS multiprocessing test suites. MMU operation was validated by running Snapgear Linux. Additional tests included an RTEMS network test application and simultaneous execution of eCos and RTEMS on different CPU nodes.

The Fault-tolerant capabilities of the system were validated by running all validation tests with GRMON error injection function enabled. The GRMON error injection function inserts errors in all LEON3-FT and GRFPU on-chip memory blocks while an application is running. GRMON's error injection model is very realistic and performed in real-time, effectively emulating an SEU testing.

7 SUMMARY

A 4-processor system based on LEON3-FT and GRFPU IP cores and satisfying the requirements on the future generation of ESA microprocessor (GINA) has been developed. The multi-processing system served as platform for verification and validation which focused on fault-tolerant and multi-processing capabilities of the LEON3-FT and GRFPU IP cores.

The fault-tolerant and multi-processing capabilities were first successfully verified by means of VHDL simulations. A FPGA board based on Virtex-4 device was developed to serve as platform for hardware and software validation. The full fault-tolerant and multiprocessor system was successfully implemented on the FPGA board on which the hardware and software validation was successfully performed.

This project has demonstrated the capability of the LEON3-FT, the GRFPU and other additional IP cores from Gaisler Research to satisfy the needs of the future generation of ESA microprocessor.

8 REFERENCES

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