SCALABLE SENSOR DATA PROCESSOR: DEVELOPMENT AND VALIDATION

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ABSTRACT

Future science and robotic exploration missions are envisaged to be demanding w.r.t. on-board data processing capabilities, due to the scarcity of downlink bandwidth together with the massive amount of data which can be generated by next-generation instruments, both in terms of data rate and volume. Therefore, new architectures for on-board data processing are in need.

The Scalable Sensor Data Processor (SSDP) is a next-generation heterogeneous multicore mixed-signal ASIC for on-board data processing, aiming at providing in a single chip the resources needed to perform data acquisition, control and high-performance processing.

This paper presents the project background and design of the SSDP ASIC. The architecture of the control and processing subsystems are presented and detailed. The current status and future development activitiess are also presented, both with prototyping and envisaged testing and validation procedures.

1. INTRODUCTION

The rates of data generated by payloads of science and robotic exploration missions are increasing due to more sophisticated and capable instruments. However, despite the growing data volume generated by payloads, the bandwidth of the down-link has not kept-up with such a growth, thus calling for more on-board data processing capabilities in order to reduce the amount of data to be transmitted. An answer to this demand comes in the form of next-generation processing architectures, capable of high-performance processing and therefore fulfilling the need of data reduction in future missions.

The Scalable Sensor Data Processor (SSDP) is a next generation mixed-signal ASIC, aiming at providing in a single chip all resources needed to perform several tasks pertaining to on-board data processing. It offers a novel heterogeneous multi-core architecture, combining two high-performance Xentium fixed-point Digital Signal Processing (DSP) cores [1] together with a LEON3FT general-purpose processor (GPP) [2], which can be used for high-performance processing and general-purpose control, including FDIR[1] functions.

The SSDP is not only about raw processing power, but also about the capability of communicating and controlling the surrounding environment, i.e. peripherals and other systems. The state-of-the-art multicore heterogeneous architecture is complemented by a diverse set of Input/Output (I/O) interfaces organized as part of a System-on-a-Chip (SoC). Available interfaces range from networked I/O like CAN and SpaceWire (SpW), to local I/O like SPI, General-Purpose I/O (GPIO), among others; to data acquisition, supporting external (off-chip) Analogue-to-Digital (ADC) and

[1] **F**ault **D**etection, **I**solation and **R**ecovery

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Digital-to-Analogue (DAC) converter, as well as high- and low-speed on-chip ADCs. Specialized I/O for control is also available, like Pulse-Width Modulation (PWM) and an on-chip DAC, together with house-keeping and time-keeping functions.

The SSDP is envisaged to be used in future scientific and robotic exploration missions like JUICE [3], having stringent requirements regarding the expected radiation environment. Its aim is easing the design, development and implementation of data processing functions, e.g. Data Processing Units (DPUs), without neglecting the control and computing capabilities offered by the GPP. The main forces driving its design are *processing power*, *power consumption* and *radiation tolerance*. The focal point of these characteristics lies between flexibility and scalability, enabling the usage of the SSDP in mission profiles so diverse as deep-space probes or planetary landers.

The SSDP builds on the experience and expertise gathered through the successful Massively Parallel Processor Breadboard (MPPB) project [4] commissioned by ESA, which aimed at developing a demonstrator of a (scalable) heterogeneous multicore DSP platform for Space applications. The mapping into ASIC technology will be performed with DARE180 digital cells. Development is sustained by a consortium led by Thales Alenia Space España, and comprising Recore Systems, IMEC, Cobham Gaisler and Arquimea, bringing together expertise in the digital, analogue and mixed-signal domains. Such diverse expertise is of the utmost importance in order to tackle the technical challenges posed by integrating the many different components, yet achieving the proposed goals.

In this paper we present the architecture, development and validation activities related to the SSDP. For that, this paper is organized in the following manner: Section 2 introduces the SSDP architecture, detailing its major subsystems and associated interfaces and peripherals; Section 3 presents the prototyping support needed by the SSDP and activities; Section 4 details the testing & validation architecture and methods; Section 5 reports the current development status and Section 6 concludes this paper.

2. SSDP ARCHITECTURE

The use cases envisaged for SSDP encompass both high-performance processing and control activities, and that is reflected in its architecture. From a bare computing architecture perspective, it is a heterogeneous multicore architecture with two different types of processors being integrated in the same die. However, it is also a System-on-a-Chip (SoC), integrating in the same die both processing resources and peripherals, which can be exploited by software.

The architecture can be roughly divided into two major subsystems, identified by their main function:

- **Control**, embodied by the Cobham Gaisler LEON3FT general-purpose processor and associated I/O interfaces, including house-keeping and system FDIR functions;
- **Processing**, embodied by Recore Systems multicore DSP subsystem, providing two Xentium DSPs and I/O interfaces, including data acquisition and conversion.

A diagram depicting the SSDP top-level architecture is shown in Figure 1, together with the functional description for the main types of I/O interfaces.

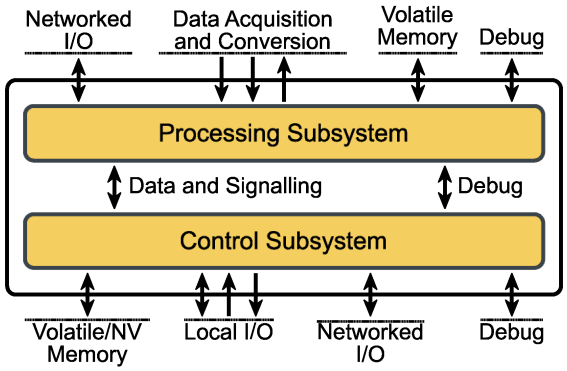

Figure 1 - SSDP Top Level Architecture

The subsystems are able to communicate internally via a high-throughput interconnect, enabling the exchange of data and signalling information between them, e.g. interrupts and debug data. Furthermore, debugging can be performed in a synchronized manner, with both subsystems being halted when one of the domains hits a breakpoint, thus enabling to capture the exact state of the entire system.

Additionally, information pertaining to EDAC errors occurring in the Processing Subsystem is forwarded to the Control Subsystem, which then can be used by the appropriate FDIR handling procedures.

Despite the names of the subsystems being tightly coupled to their function and available functional I/O units, each of them is capable of implementing and/or using functions of the other – up to some extent. For example, the Control subsystem can use some of its features to perform processing functions and vice-versa.

2.1. Processing Subsystem

The bulk of the Processing Subsystem is encapsulated by RECORE's multicore DSP IP. This IP provides two Xentium fixed-point DSPs [1] together with local memories and several functional units (modules),

providing I/O activities and data acquisition & conversion capabilities. These modules are interconnected via a highly performing Network-on-a-Chip (NoC), with each one possessing a Network Interface (NI) which is used to exchange packets with other modules over the NoC, via routers. A block diagram of the Processing Subsystem is presented in Figure 2.

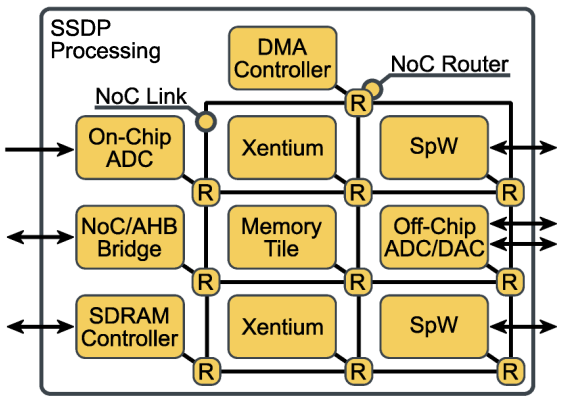

Figure 2 - SSDP Processing Subsystem Block Diagram

NoC links are 32-bit wide and capable of executing one transfer per clock cycle, thus yielding a maximum bidirectional throughput of 3.2 Gigabit per second. Packet exchange is performed with routers via a 2D mesh, with the paths being defined as X and Y coordinates. Link contention at router level is addressed by serving the links in a round-robin fashion.

Regarding I/O interfaces, the Processing Subsystem can make use of SpW interfaces to exchange data with external systems. Local I/O can be performed via the Data Acquisition & Conversion interfaces, for external devices. Data exchange with the Control Subsystem is performed via a NoC-to-AHB bridge, together with signalling and EDAC error information.

Processing Resources and Profiling

The Xentium DSP provides the processing resources for the Processing Subsystem. It is a 32-bit fixed-point VLIW[2] architecture, having a datapath with many functional units which are capable of executing operations in parallel, namely:

- 4x 16-bit Multiply-Accumulate Operations (MACs)
- 2x 16-bit Complex MACs
- 2x 32-bit MACs

The datapath is connected to banked 32 kB low-latency Tightly-Coupled Memories (TCMs), and capable of performing four 32-bit load/store operations per clock cycle, thus enabling the implementation of high-throughput algorithms which can exploit the aforementioned datapath resources.

Application program code is stored in a dedicated cache memory with a 16 kB size. Profiling of application can be performed efficiently due to the provision of event counters at hardware level, which store many metrics related to application execution, like cache hit-rate among others.

Memory Hierarchy and DMA

The storage of (volatile) data is performed through a hierarchy of memories, ranging from low-latency TCMs to high-capacity (512 MB) external SDRAM at 100 MHz. A shared 64 kByte SRAM-based Memory Tile is embedded in the Processing Subsystem and connected directly to the NoC, which can be used as an intermediate memory between the TCMs and the SDRAM.

Data exchange can make use of a dedicated Direct Memory Access (DMA) controller, providing up to 8 concurrent transfers which can be programmed either by the Xentium processors or the LEON3FT on the Control Subsystem. The controller can also perform *stride-based* transfers, i.e. picking only one of every *m* data on a set with *n* elements (e.g. I/Q samples processing or decimation functions without DSP intervention). Furthermore, transfers can be performed in 2D, further enabling the efficient transfer of data inside the SSDP.

Data Acquisition & Conversion and System Scaling

Data acquisition can be performed both using off- and on-chip ADC, up to 16-bit per sample. Dedicated interfaces for external data acquisition and conversion devices (ADCs and DACs) are available, including the possibility of device multiplexing. Maximum sample rate for external devices is 50 Msps, whilst the on-chip ADC sample rate can go as high as 100 Msps. Data can be pre-processed at low-level, after acquisition, with functions like averaging being performed at the acquisition interface of the SSDP.

Scaling of SSDP-based systems has been envisaged, and with that purpose a Chip-to-Chip (CtC) interface has been introduced in order to connect the SSDP with other devices – be it SSDP chips, FPGAs or other companion devices. This full-duplex parallel interface has a 16-bit width, and is capable of exchanging data at a speed up to 50 MWords per second, yielding a maximum throughput of 800 Mbps. The interface has hardware-based flow-control mechanisms, thus enabling reliable communication support.

[2] **V**ery **L**arge **I**nstruction **W**ord

Summary

The Processing Subsystem provides a high-performance multicore DSP SoC, having also data acquisition and storage capabilities. Its most striking features are:

- Multicore 32-bit fixed-point VLIW DSP (x2)
- 3.2 Gbps NoC interconnect
- Internal 64 kB SRAM, external SDRAM
- SpW with RMAP target, up to 200 Mbps
- On-chip ADC up to 100 Msps
- Off-chip ADC and DAC up to 50 Msps
- Chip-to-Chip Interface, up to 800 Mbps

These features can be efficiently exploited by application designers through compilers and a graphical Software Development Environment, with debugging capabilities.

2.2. Control Subsystem

At the heart of the Control Subsystem there is a SoC based on the flight-proven Cobham Gaisler LEON3FT, a fault-tolerant SPARC V8 architecture. The SoC modules are interconnected via a shared 32-bit ARM AMBA 2.0 bus, yielding a maximum throughput of 3.2 Gbps. A block diagram depicting the Control Subsystem and its components is shown in Figure 3, with the remaining SoC components.

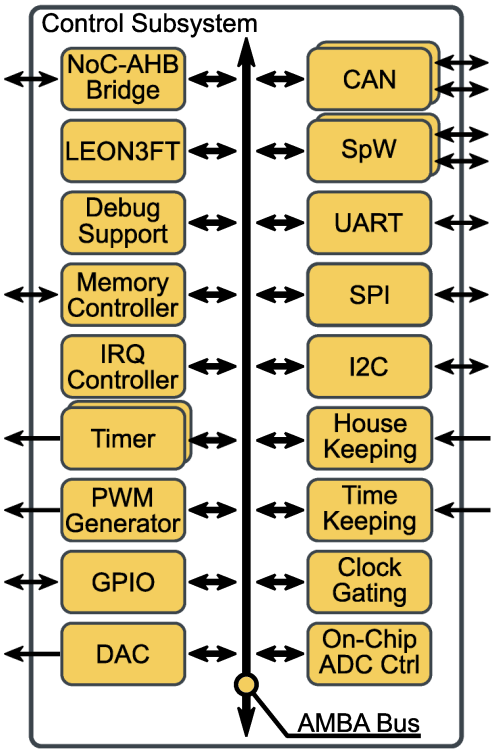

Figure 3 - SSDP Control Subsystem Block Diagram

Most of the modules of the Control Subsystem are provided by the Cobham Gaisler GRLIB, and have been flight-proven in previous successful ASICs like the UT699 or the GR712RC. However, some new modules have been added by TAS-E to implement functions not available in GRLIB, such as House-Keeping or current DAC control.

Since the main scope of this subsystem is control, the set of I/O peripherals has to support the processing unit in fulfilling its mission. Both local and networked I/O interfaces are available, thus allowing the communication and control of both local and remote systems and devices. Such interfaces range from SpW and CAN to local device control with SPI or I2C. Furthermore, there are interfaces dedicated to directly interface with actuators such as brushless motors, e.g. Pulse-Width Modulation (PWM) outputs. Clock gating is available, allowing to save power by turning-off unused modules, including ones present on the Processing Subsystem.

Analogue I/O interfaces also exist, such as an on-chip high-precision 12-bit low-speed (<60 ksps) current DAC. This DAC can be used for multiple purposes, ranging from thermistor current reference, e.g. Pt1000 probes, to generate bias currents for other devices. Furthermore, it can also be used to control devices with the help of additional electronics, e.g. current-to-voltage converters. The DAC interface is complemented by a low-speed ($\leq$ 833 ksps) voltage ADC intended primarily to be used in house-keeping activities, but also capable of being used in other applications.

Processing Resources and Operating System Support

The LEON3FT processor implements the well-known SPARC V8 Instruction Set Architecture, providing the general-purpose processing support for the SSDP Control Subsystem. Nevertheless, it is endowed with advanced features and mechanisms, in order to enhance the processing performance:

- High-performance IEEE-754 compliant Double Precision Floating Point Unit (FPU);
- Hardware Integer Multiplication and Division
- Separate 4-way set-associative 16 kB Data and Instruction cache memories;

Furthermore, is possible to lock lines of instruction cache, allowing to speed-up the execution of some portions of code by reducing latency, e.g. fast interrupt-handling routines.

Operating system (OS) support is provided, via timer units, interrupt controller and even a Memory Management Unit (MMU). Such components allow running both Real-Time Operating Systems (RTOS)

like RTEMS, or modern generic operating systems like Linux. A Debug Support Unit is provided for on-ground application development with standard Cobham Gaisler tools like GRMON together with profiling mechanisms.

Memory Support

The storage and execution of software applications is supported by a Fault-Tolerant Memory Controller supporting both non-volatile (mature PROM, EEPROM and novel MRAM) and volatile (SRAM) memory technologies. Furthermore, these can be protected by Error Detection and Correction (EDAC) mechanisms in order to ensure reliable operation in the harsh space environment.

House-keeping and Time-keeping & distribution

House-keeping capabilities have not been neglected in the SSDP, and are supported by an on-chip low-speed (≤ 833 ksps) voltage ADC. The device is capable of measuring several internal parameters of the ASIC, e.g. internal supply voltage or temperature. Up to 64 multiplexed external parameters (voltages) can be measured.

Time-keeping services are also provided by the Control Subsystem, and complemented by either Spacecraft or Instrument own services. Time distribution is managed by the novel SpaceWire Time Distribution Protocol (SpW-TDP) [5], whose IP core has been enhanced with time-keeping and management functions. Besides the presence of SpW-TDP, local time distribution and synchronization is also possible via dedicated input pins, e.g. Pulse Per Second (PPS).

Summary

The Control Subsystem offers many resources which enable its exploitation as a fully capable On-Board Computer (OBC) component, with emphasis on control but without neglecting processing tasks:

- LEON3FT with FPU and Cache Memories
- Networked I/O: CAN, SpW
- Local I/O : GPIO, SPI, I2C, among others
- EDAC-protected Memory Storage
- Timer Units, IRQ Controller, MMU
- House-keeping, Time-keeping and distribution

The architecture of the Control Subsystem is intended to be highly compatible with the commercially available GR712RC GPP from Cobham Gaisler [6], which is also based on the LEON3FT. The objective of such compatibility is to allow the reuse in the SSDP of code, tools and procedures already developed for the GR712RC and its applications.

3. PROTOTYPING SUPPORT

A prototyping platform is required in order to be able to perform test and validation activities. Such platform must be capable of supporting the prototyping activities of the ASIC RTL, usually resorting to FPGAs, and at the same time to be representative of the envisaged I/O interfaces. A block diagram with the architecture of the prototyping platform is shown in Figure 4

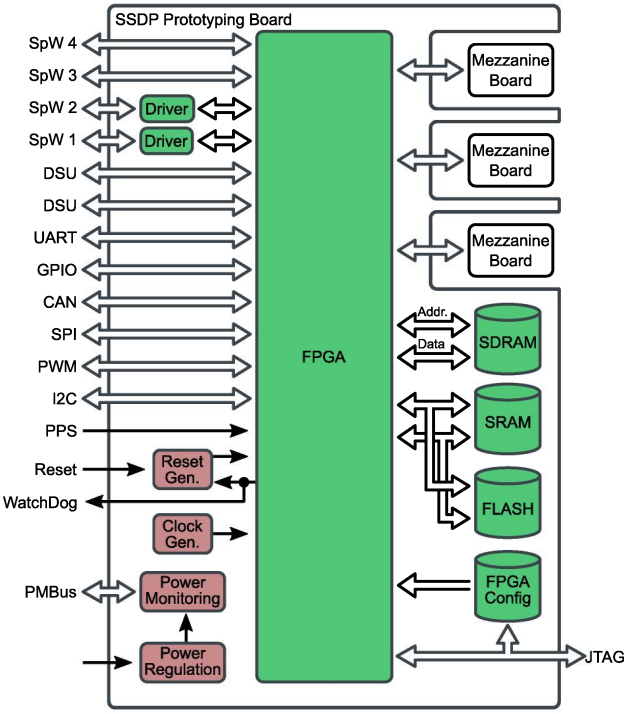

Figure 4 – SSDP-PROB FPGA Prototyping Board

In order to be able to accommodate the RTL of both subsystems, the FPGA device is a state-of-the-art Xilinx Kintex Ultrascale XCKU060 [7]. Mezzanine connectors based on the FMC standard were added, enabling the expansion of the board with modules such as an ADC or DAC, as well as allowing the probing of internal signals. The resulting printed-circuit board named SSDP Prototyping Board (SSDP-PROB) is shown in Figure 5.

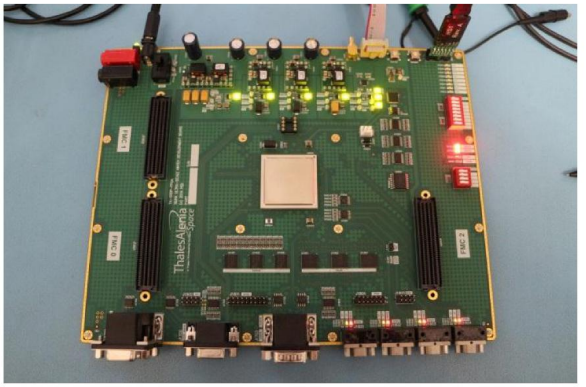

Figure 5 – SSDP-PROB - SSDP Prototyping Board

4. TEST AND VALIDATION

The test and validation of a sophisticated device like the SSDP encompasses several tasks, at different levels of abstraction. Some of the activities are:

- *Module testing*, where each of the modules – be it I/O or other function – are tested, usually against a specification or standard;
- *Validation,* where a set of modules is used in order to prove that a certain function or set of functions are working;
- *Benchmarking*, where some standard but especially crafted procedures are executed, and the result – be it time or another metric – is measured, and then compared with the execution of the same procedures on other systems.

On the SSDP we will make use of the three methods, which will allow performing test and validation of the ASIC. However, the execution of test and validation procedures requires a properly defined architecture for testing, mapped into a test setup and encompassing hardware and software components.

4.1. Test Setup

Testing and validation is usually performed by having a test bench driving the testing activities, providing stimuli to a Unit Under Test (UUT) and then observing the outputs. Correctness is assessed by comparison with a given reference, which can be based either on specifications of I/O interfaces, or output of reference applications and algorithms.

The first step towards test and validation activities was described previously, with the definition and implementation of a (hardware) prototyping platform. With the prototyped SSDP being the UUT, some sort of Electrical Ground Support Equipment (EGSE) is needed as the test bench, in order to provide the necessary stimuli (I/O activities), and capture the outputs for verification. This architecture is depicted in the block diagram of Figure 4.

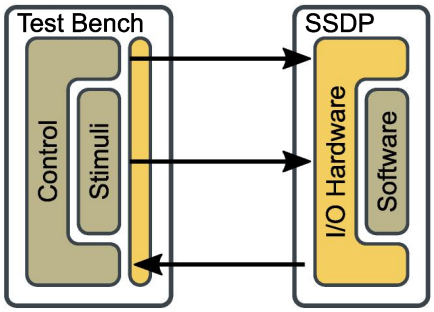

Figure 6 – SSDP Testing Architecture Block Diagram

Furthermore, some software will also be needed, in order to implement the testing and validation activities, both on the SSDP and EGSE sides.

The test setup for SSDP requires an integrated and flexible EGSE platform, given the diversity and amount of I/O interfaces. Such a platform is embodied by the National Instruments (NI) PXI, offering the possibility to embed in a single chassis the controller cards and I/O interfaces, including digital reconfigurable I/O for both stimuli and control. The hardware setup to be used to test and validate the SSDP ASIC is shown in Figure 8.

Figure 7 – SSDP EGSE Setup for Testing

Such platform is controlled with LabView, an industry standard software w.r.t. testing design and execution. Testing activities running on the Test Bench are modelled as LabView applications, and software shall be running also on the SSDP. The resulting overall architecture is depicted in Figure 8.

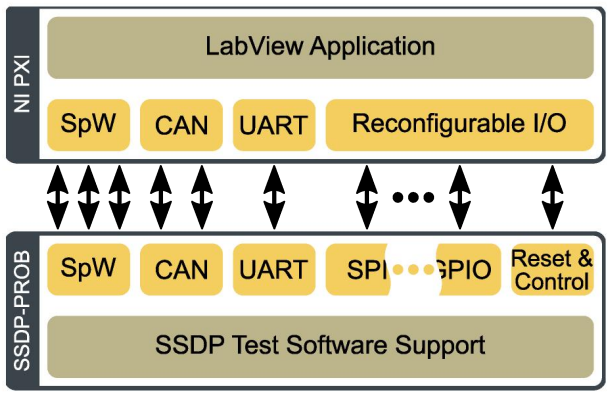

Figure 8 – SSDP Test Setup Architecture

This generic architecture shall be used by all the needed testing and validation activities. Although the Test Bench will always be in charge of the testing and validation activities, the division of the software test effort between the Test Bench and the SSDP prototype is dependent on the type of activities, as described in the next sections.

4.2. Module Testing

The testing of the SSDP modules is a crucial task to ensure their adherence to the specification. All the I/O interfaces of interest present on the board are connected to the test bench, using adequate EGSE I/O cards. Some of the interfaces which cannot be (directly) tested, such as the analogue part of ADCs and DACs, have their digital part emulated. For instance, the digital I/O card present on the Test Bench can be used to cyclically output digital words compatible with the ones output by the digital part of the ADC.

Interaction between the Test Bench and SSDP require some sort of software support on the SSDP side. Communication is performed via a specific interface using a set of pre-defined tele-commands (TCs). The TCs can be used to perform the following actions on the SSDP: setup interfaces; initialize memory areas and patterns; start and stop tests.

In this specific case, the Test Bench software (LabView) is the one performing the bulk of the testing activities, providing both stimuli and control, and relying on (some) software support present on the SSDP. Such implementation stems from the extremely low-level nature of modules, and the need to have some abstraction, which is given by the SSDP support software. Such support is provided mostly in the form of peripheral drivers.

4.3. Validation

Validation activities are performed at a higher-level of abstraction, where an application exploits several modules in order to provide a specific function. An example of such is an operating system, a compression algorithm or image processing. The execution of these is compared with reference models and/or outputs, in order to assess their correctness.

These activities require more support from the software running on the SSDP itself, i.e. applications. The Test Bench is then used as an emulator of the environment where the application is envisaged to work, e.g. instrument or mass memory, for on-board processing activities.

In the scope of the SSDP validation activities, some of the envisaged applications to be used are:

- Image processing, with edge-detection algorithms;
- Compression, with algorithms such as CCSDS 122;
- Operating System support, like RTEMS.

These are not the only applications to be used as validation; they were selected for their ability to represent real SSDP use-cases.

4.4. Benchmarking

The (raw) performance of the SSDP has to be assessed and characterized, in order to be able to be compared with other solutions and support the decision-makers upon deciding which device or architecture to use in a given project. Benchmarking is the method used to obtain standard performance metrics for a given figure of metric in a given system, which can then be compared with results obtained on other systems.

Benchmarking activities require the use of especially crafted tests, whose execution will be timed in order to provide a reference. An example of such a set of tests is ESA NGDSP benchmark [8], which will be used to assess the performance of the Processing Subsystem. These activities will depend mostly on software implemented in the SSDP, with the Test Bench providing (few) stimuli.

5. DEVELOPMENT & STATUS

The SSDP is being developed through an industrial consortium led by **Thales Alenia Space España** (ES), and encompassing several partners across Europe with different domains of expertise:

- **Recore Systems** (NL), providing the multicore DSP and components of the Processing Subsystem, together with the Software Development Environment (SDE) and support;
- **Cobham Gaisler** (SE), with the LEON3FT SoC and support;
- **IMEC** (BE), providing specific IP cores, DARE180 cell library, and also the layout services, package, assembly support, foundry interface and manufacture testing;
- **Arquimea** (ES), with the on-chip fast ADC.

The SSDP development will result in a CQFP-352 mixed-signal ASIC, built in UMC 180 nm technology with DARE180 digital cell technology [9], capable of working with a clock frequency of up to 100 MHz. The radiation performances of the ASIC are expected to compatible with the harsh environment of science and robotic exploration missions, based on previous developments based on the UMC 180 nm technology, including latch-up tests of analogue blocs. A TID[3] of at least 300 krad (Si) is envisaged, which could be up to 1 Mrad (Si) based also on previous ASICs' radiation testing results.

[3] **T**otal **I**onising **D**ose

The SRR was successfully closed out in October 2015, and the current activities related to development and subsystem integration will culminate with a PDR in 2016. The current schedule for the following (major) milestones is the following:

- Q1 2017 – CDR
- Q2 2017 – Prototypes Manufacturing
- Q3/Q4 2017 – Prototypes (EM) Available
- 2018 – FM Available

Evaluation boards with EMs are expected also during H2 2017, after the testing and validation campaign. Engineering Models (EMs), Flight Models (FMs) and evaluation boards will be commercialized by Cobham Gaisler.

6. CONCLUDING REMARKS

The Scalable Sensor Data Processor (SSDP) is a next-generation data processing mixed-signal ASIC, providing in a single package a sophisticated heterogeneous multicore architecture with a Processing Subsystem equipped with powerful multicore DSP processing capabilities, together will a Control Subsystem using well-established general-purpose processing resources capable of delivering fast and reliable control and house-keeping functions.

Besides the powerful Xentium Processors, the Processing Subsystem is supported by a high-performance Network-on-Chip (NoC), interconnecting the processing resources with SDRAM storage, I/O such as SpW and on- and off-chip data acquisition for ADCs and DACs. A Chip-to-Chip interface is also provided, allowing scaling a system with other devices, such as additional SSDP ASICs, FPGAs or others.

The Control Subsystem offers a general-purpose LEON3FT with a floating-point unit, together with SpaceWire, CAN and local I/O such as SPI and I2C, and capable of performing house-keeping and time-keeping & distribution activities. It is highly compliant with the LEON3FT-based Cobham Gaisler GR712RC SoC, thus allowing the efficient porting of applications developed for that platform to the SSDP.

The SSDP RTL is currently being integrated, tested and validated by using a custom FPGA-based prototyping board based on the Xilinx UltraScale architecture, and versatile test bench hardware & software based on NI PXI and LabView.

The next step after validation will be to perform the ASIC layout. The SSDP ASIC will be implemented in UMC 180 nm technology, using DARE180 digital cells, providing it a high degree of SEE tolerance which is in line with envisaged future science and robotic exploration missions. The first prototypes for testing and validation are expected to be delivered during the second half of 2017, with evaluation boards being made available by Cobham Gaisler.

REFERENCES

[1] Recore Systems, “Xentium® VLIW DSP IP Core - Product Brief,” 2016. [Online]. Available: http://www.recoresystems.com/fileadmin/downloads/Product_briefs/2016-1.0_Xentium_Product_Brief.pdf.

[2] Cobham Gaisler, “GRLIB IP Core User's Manual,” April 2016. [Online]. Available: http://www.gaisler.com/products/grlib/grlib.pdf.

[3] European Space Agency, “JUICE Definition Study Report,” 2014.

[4] Recore Systems, “Massively Parallel Processor Breadboarding Study,” 2012.

[5] Cobham Gaisler, “High Accuracy Time Synchronization over SpaceWire Networks,” 2013.

[6] Cobham Gaisler, *GR712RC Dual-Core LEON3-FT SPARC V8 Processor,* 2016.

[7] Xilinx Inc., *UltraScale Architecture and Product Overview,* 2016.

[8] TEC-EDP/2008.18/RT, “Next Generation Space Digital Signal Processor Software Benchmark,” ESA, 2008.

[9] S. Redant, R. Marec, L. Baguena, E. Liegeon, J. Soucarre, B. Van Thielen, G. Beeckman, P. Ribeiro, A. Fernandez-Leon and B. Glass, “The Design Against Radiation Effects (DARE) Library,” in *5th Radiation Effects on Components and Systems Workshop (RADECS)*, Madrid, 2004.